REMARKS

Claims 10-13 are pending herein.

I. The anticipation rejections based on Okabe (US 7,154,454).

The USPTO respectfully rejects claims 1-13 under 35 U.S.C. § 102(e) as being allegedly anticipated by Okabe. Claims 1-9 have been cancelled. Claims 10 and 11 are independent claims.

A. Okabe does not disclose that the first write control transistor and the second write control transistor are connected to a single data line, as claimed in claim 1.

Claim 10 claims in relevant part:

> "a first write control transistor having a first region connected to a connection portion between the driver transistor and the drive current control transistor and **a second region connected to ~~the~~ a data line**;
>
> a second write control transistor having **a first region connected to the data line** and a second region connected to the gate of the driver transistor." **(emphasis added)**

No new matter is added by the amendment, as the amendment merely corrects an antecedent basis issue. Regarding these limitations, it is respectfully not seen where Okabe discloses the claimed structure quoted above.

Specifically, the USPTO respectfully alleges on page 6 of the Office Action that elements 8 and 4 of Okabe are the specifically claimed first and second write control transistors of claim 10. However, it is respectfully important to note that **transistors 8 and 4 of Okabe are not connected to the same data line, as claimed in claim 10.** Instead, transistor 4 of Okabe has one end connected to luminance data line 3, and transistor 8 of Okabe has connections to point d, control signal line 9, and point g, as seen in present Figure 1. It is respectfully important to note that, **in Okabe, no region of transistor 8 connects to luminance data line 3.** Thus, transistors 8 and 4 of Okabe do not have regions connected to the same data line, as claimed in claim 1.

Additionally, there is no "common sense" reason or other motivation to modify Okabe so that transistor 8 and transistor 4 would each have a region connecting to the same data line. For example, transistor 8 of Okabe only has the function of short-circuiting the gate and drain of transistor 7 when it is turned on, and it is respectfully asserted that transistor 8 of does not have any function similar to that of the first write control transistor of Okabe. **Thus, according to the disclosure of Okabe, it would not make technical sense for transistors 8 and 4 to share the same data line.** Therefore, there is no "common sense" reason to modify Okabe in this way.

In contrast, present Figure 3 illustrates one possible embodiment of the claimed structure quoted above. As clearly seen in present Figure 3, transistor 18 (i.e., a first write control transistor), has a region connected between transistors 10 and 12, and a region connected to data line DL1. Additionally, present Figure 3 shows that transistor 16 (i.e., a second write control transistor) has a region connected to the gate of transistor 10, as well as a region connected to data line DL1. It is respectfully important to note that **both transistors 16 and 18 have regions connected to the same data line DL1.** Thus, transistors 16 and 18 are one possible example of the specifically claimed first and second write control transistors, as claimed in claim 10.

Thus, it is respectfully asserted that Okabe does not disclose all of the limitations of claim 10. Therefore, it is respectfully asserted that Okabe does not anticipate claim 10, and claim 10 is therefore allowable.

B. Further explanation regarding claim 10.

Regarding claim 10, Applicants further respectfully note that with the structure described in Okabe, it is impossible to perform the function of turning on the first write control transistor when a "data current signal" is supplied to the data line so that the data current signal flows to the data line through the driver transistor and the first write control transistor.

Additionally, Okabe also does not disclose that a "data voltage signal" and a "data current signal" are supplied to the data line, and does not describe the necessity of supplying a data current signal. Also, if it is assumed that a current flows to the data line and, in response

to that, the transistor 8 of Okabe is controlled to turn on, it is completely impossible to flow the data current signal to the data line through the transistors 7 and 8 of Okabe. It should be noted that, if the transistor 4 is additionally controlled to turn on in the above case, it is impossible to flow a current to the data line through the transistor 8 because a capacitor 5 is provided between the transistor 4 and the transistor 8.

C. Okabe does not disclose that each of a plurality of data lines is provided corresponding to each column of the matrix and a different data line among the plurality of data lines is connected to corresponding pixels for each row of the matrix, as claimed in claim 11.

Claim 11 claims in relevant part:

> "each of **a plurality of data lines is provided corresponding to each column of the matrix** and **a different data line among the plurality of data lines is connected to corresponding pixels for each row** of the matrix." **(emphasis added)**

Regarding these limitations, it is respectfully not seen where Okabe discloses the claimed structure quoted above.

Specifically, the USPTO respectfully alleges on page 7 that column 1, lines 57-67 and Figures 1 and 9 of Okabe disclose the specifically claimed plurality of data lines, as claimed in claim 11. However, it is respectfully asserted that **Okabe does not teach or suggest anything about a matrix of pixels, or a plurality of data lines being provided for each column of a matrix of pixels**, as claimed in claim 11. For example, it is respectfully noted that Okabe only allegedly shows a single data line 3 in the Figures, and does not show a plurality of data lines. Thus, it respectfully follows that Okabe cannot teach or suggest that such a plurality of data lines is provided for each column in a matrix, as claimed in claim 11.

Additionally, it is respectfully asserted that in Okabe, it is impossible that, for each row, a different data line in the plurality of data lines is connected to a corresponding pixel in this column.

In contrast, present Figure 3 illustrates one possible embodiment of the claimed structure quoted above. Specifically, present Figure 3 shows two pixels in a column. Additionally, **there is a plurality of data lines (i.e., data lines DL1 and DL2) provided for the column of pixels in present Figure 3**, as claimed in claim 11. As further seen in present

Figure 3, data line DL1 is provided for the top pixel, and data line DL2 is provided for the bottom pixel. Thus, **there is a different data line provided to each row of pixels**, as claimed in claim 11.

Thus, it is respectfully asserted that Okabe does not disclose all of the limitations of claim 11. Therefore, it is respectfully asserted that Okabe does not anticipate claim 11, and claim 11 is therefore allowable.

D. The dependent claims.

As noted above, it is respectfully asserted that independent claim 11 is allowable, and therefore it is further respectfully asserted that dependent claims 12-13 are also allowable.

II. Conclusion.

Reconsideration and allowance of all of the claims is respectfully requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Please contact the undersigned for any reason. Applicants seek to cooperate with the Examiner including via telephone if convenient for the Examiner.

Respectfully submitted,

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